



Inventor: Dean Nobunaga
FAST DATA ACCESS MODE IN A MEMORY DEVICE
Atty Docket No. 400.239US01 Serial No. 10/613,119

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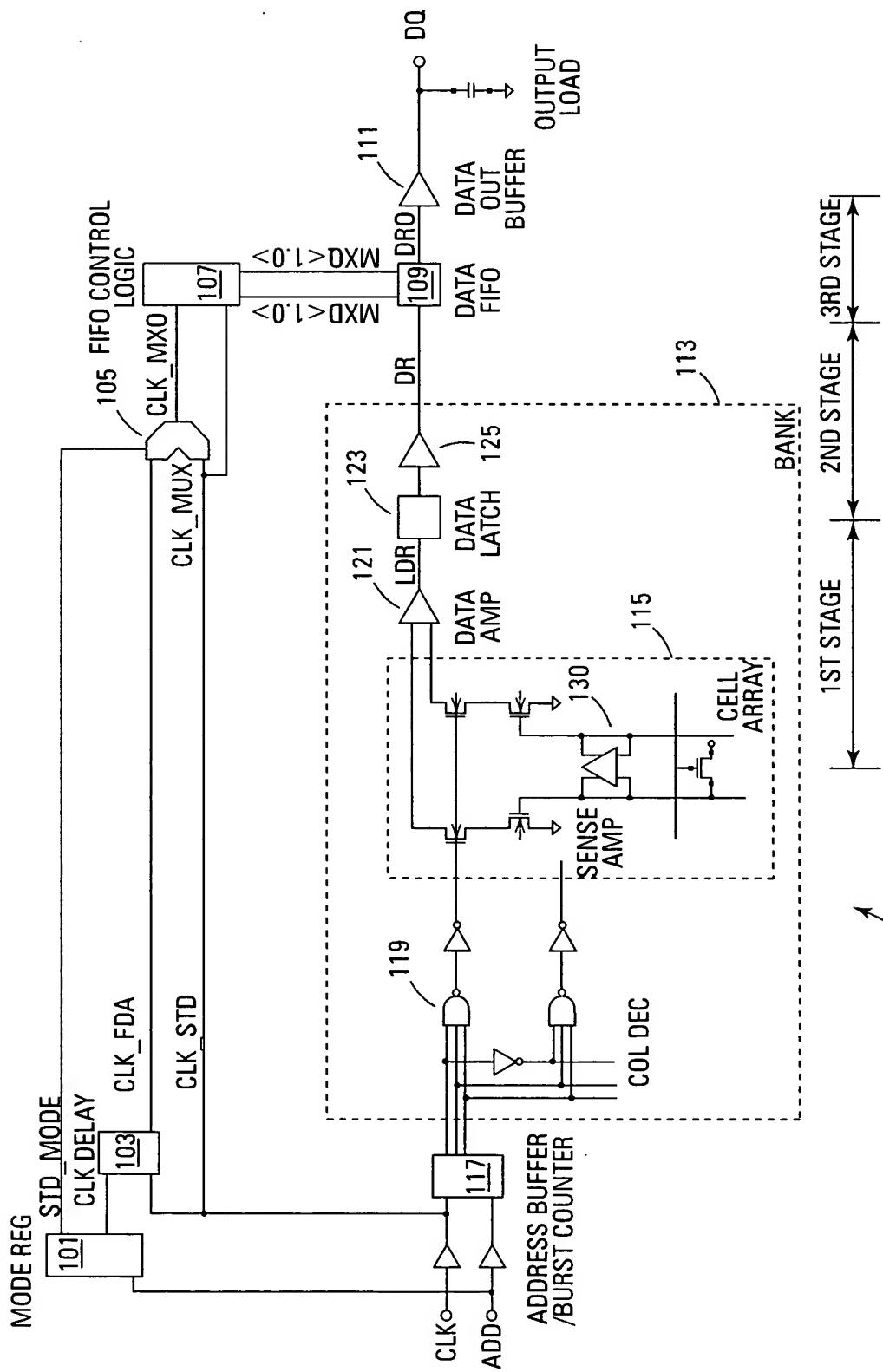


Fig. 1



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CLK FREQ	WB	OP MODE	CAS LATENCY	BT	BURST LENGTH	DESCRIPTION						
M11	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	M0	
												Burst1
												Burst2
												Burst4
												Burst8
												Reserved
												Reserved
												Reserved
												Full Page
												0
												Sequential
												Interleaved
												Reserved
												Latency1
												Latency2
												Latency3
												Reserved
												Reserved
												Reserved
												Standard Operation
												Fast TAC Mode
												Reserved
												Reserved
												Programmed Burst Length
												Single Location Access
												143MHz
												166MHz
												200MHz
												250MHz

Fig. 2

Patent
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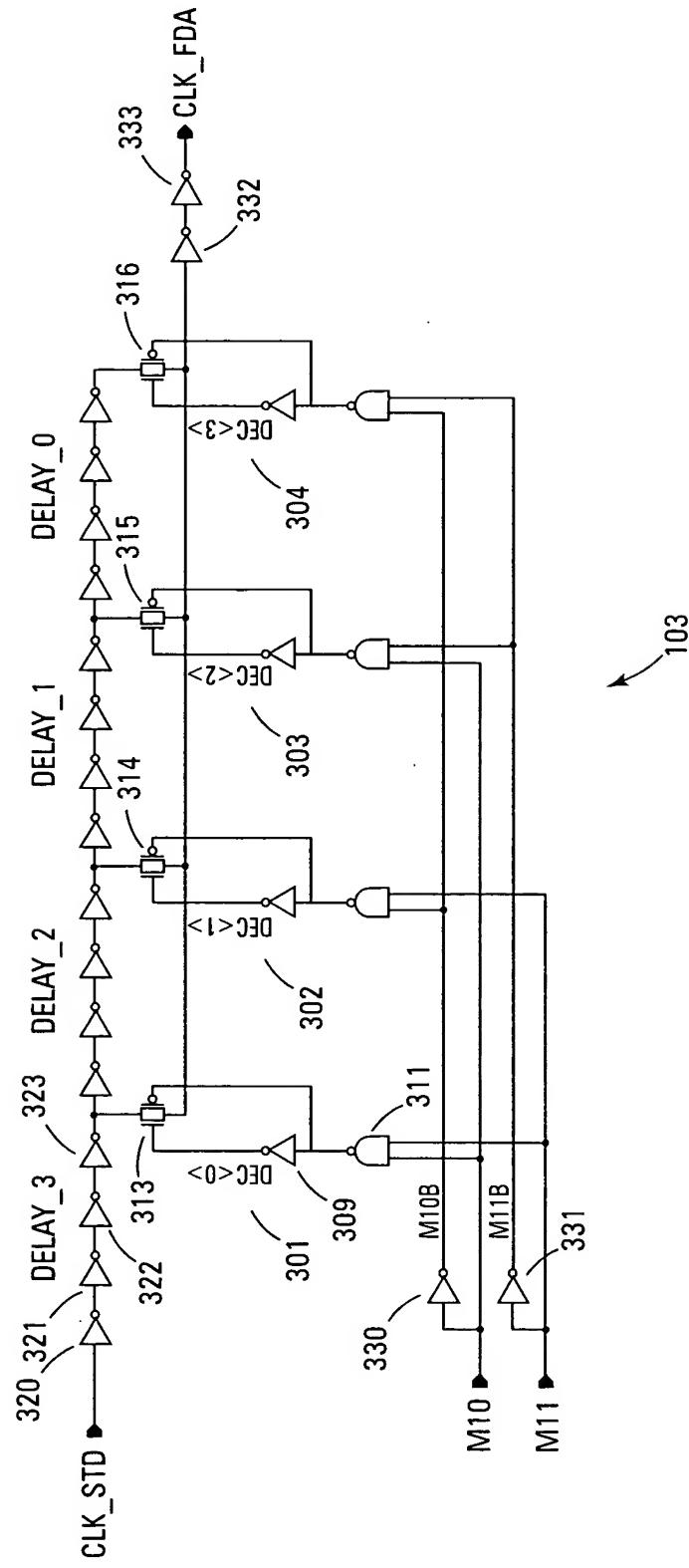


Fig. 3



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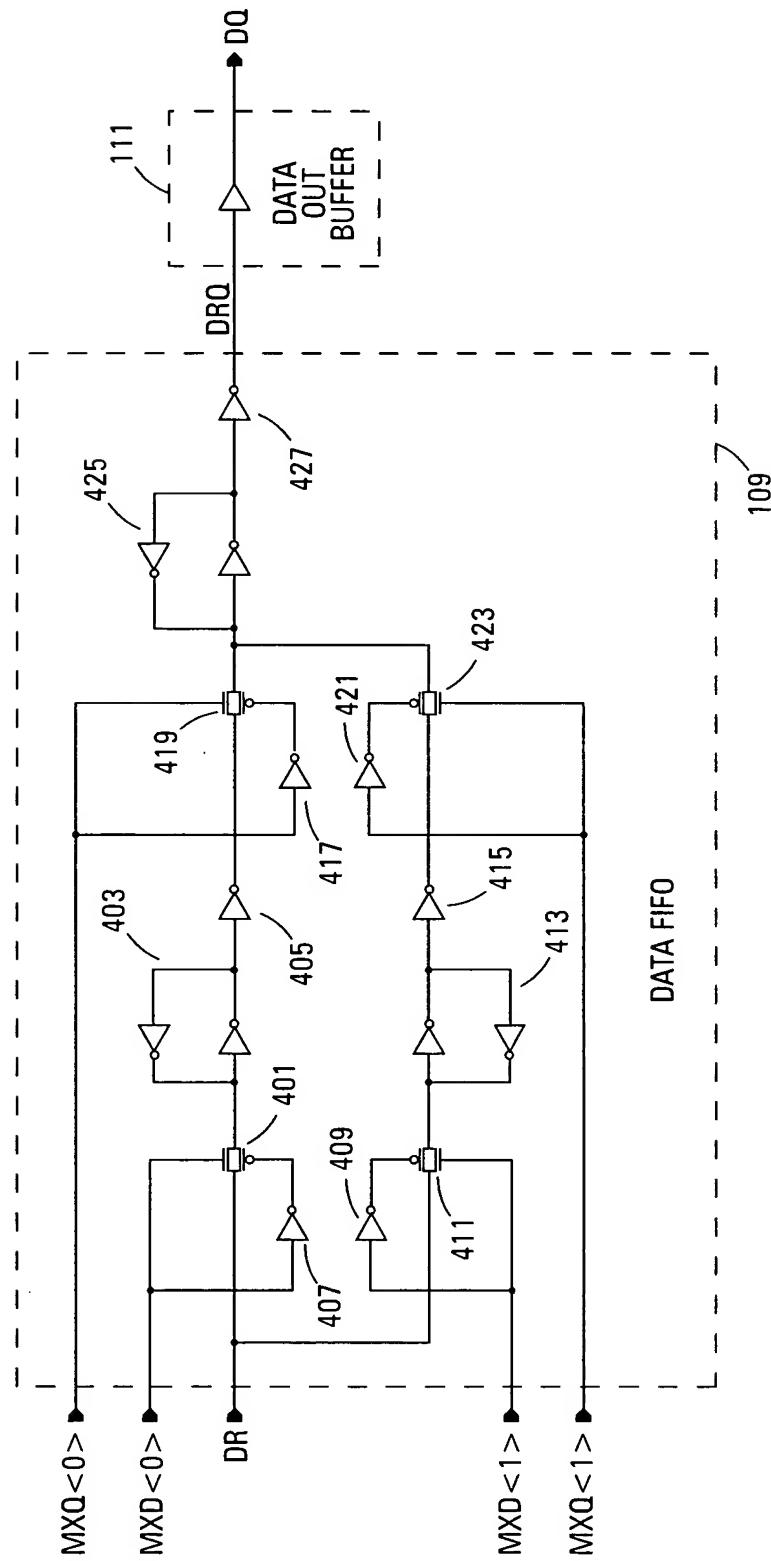


Fig. 4

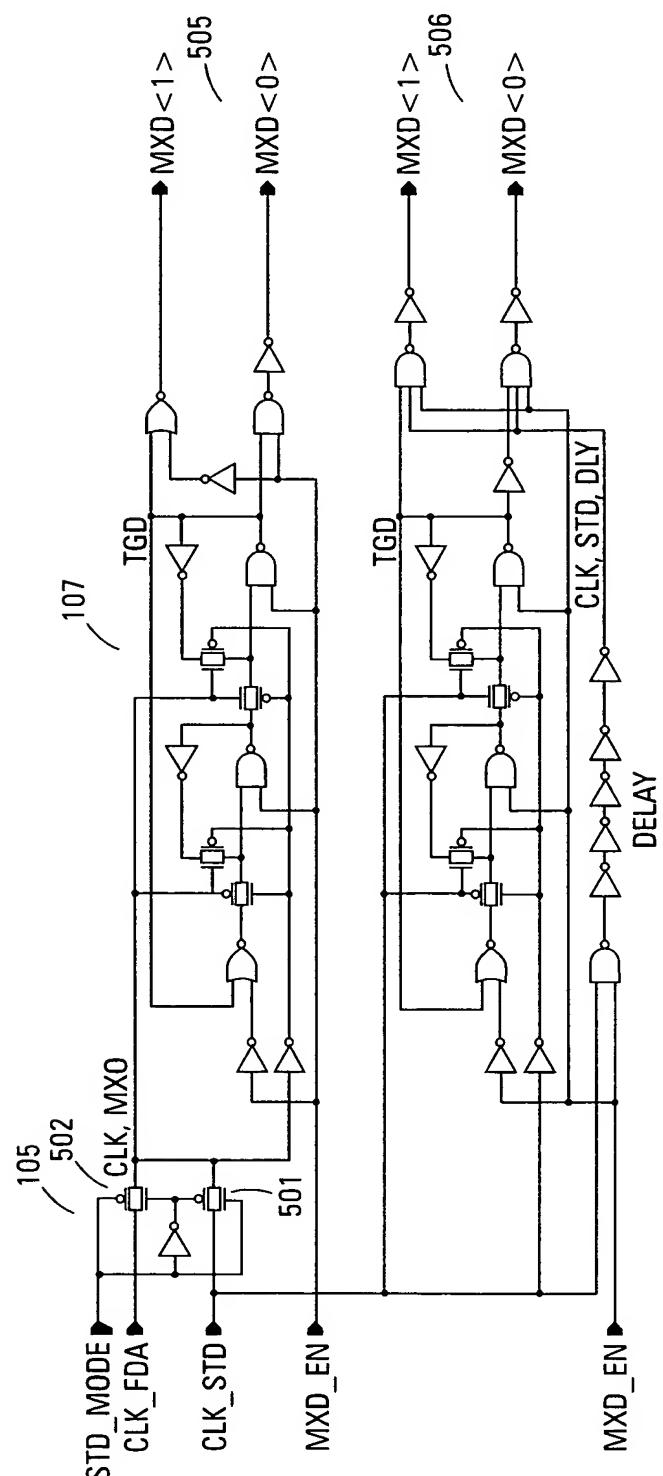


Fig. 5

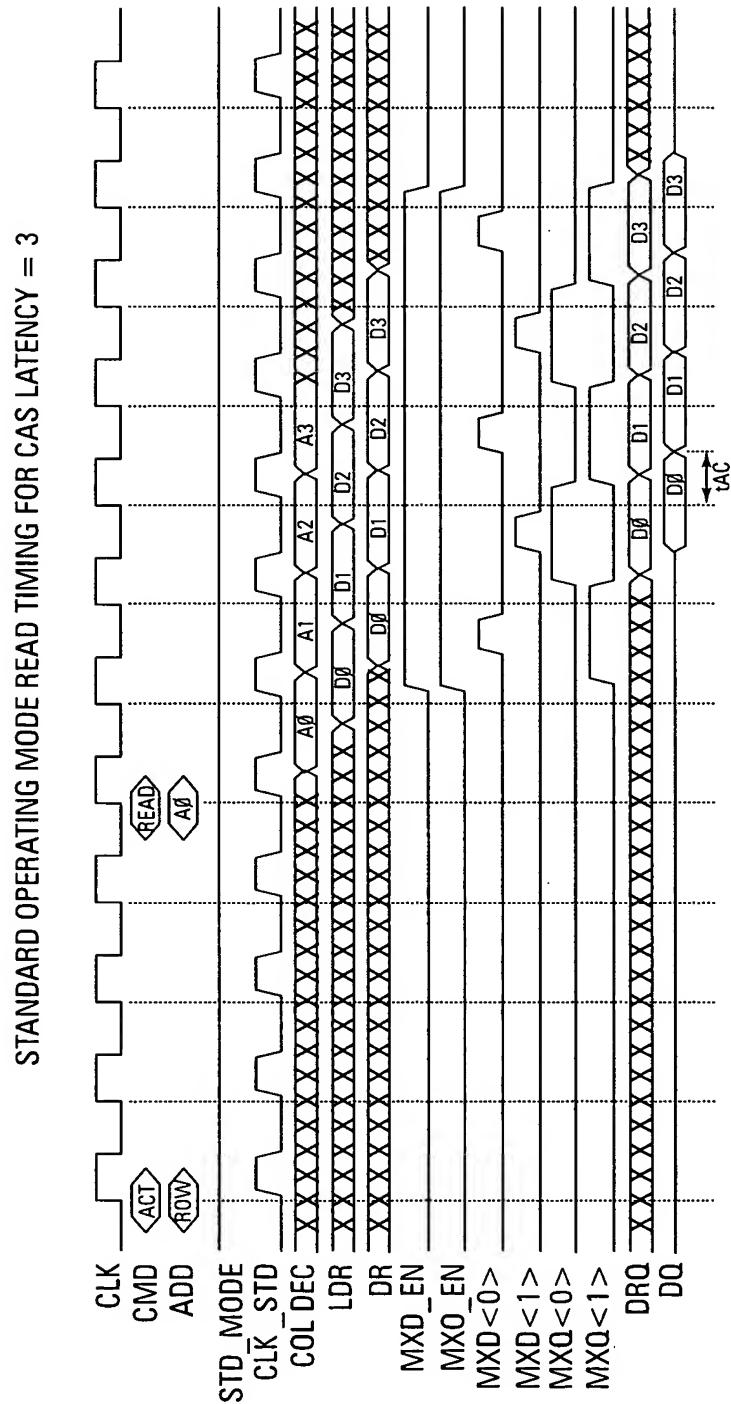


Fig. 6

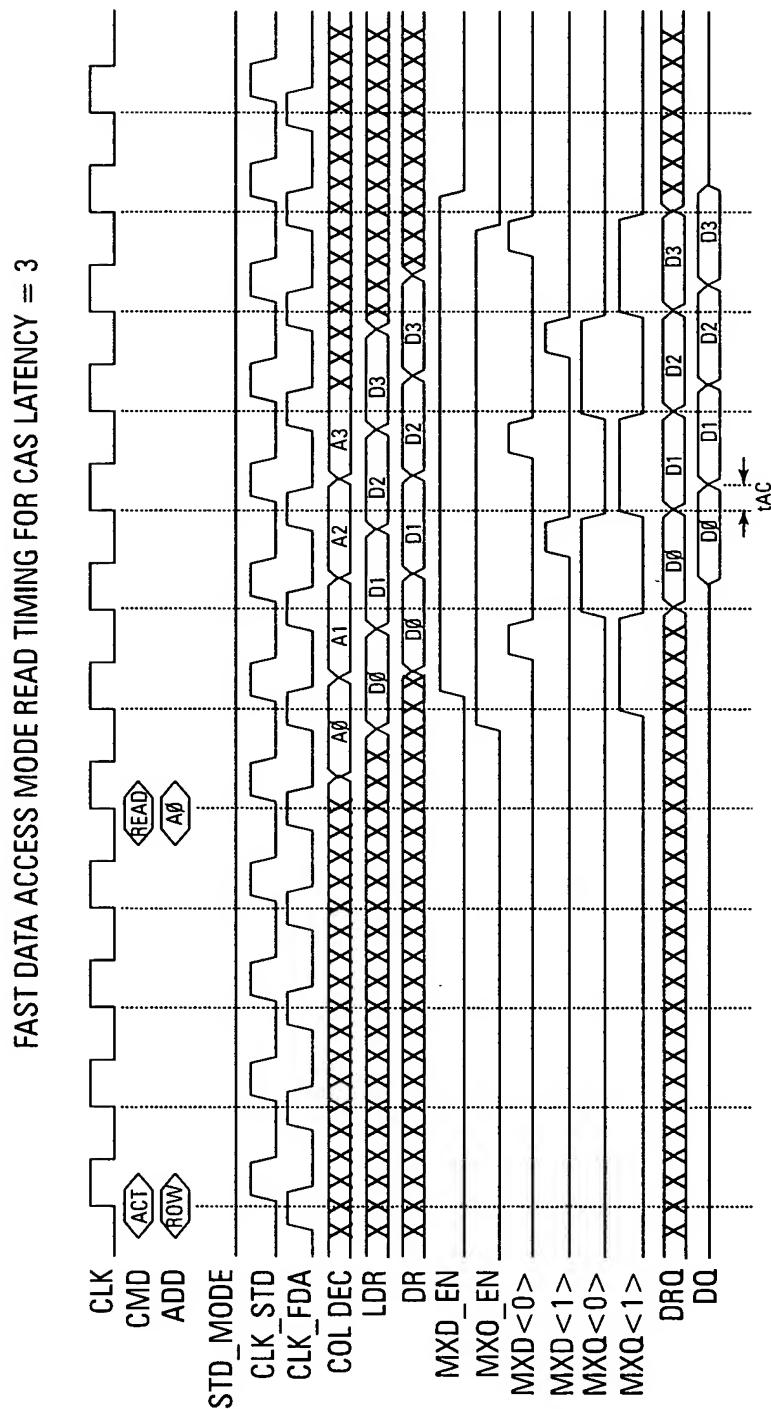
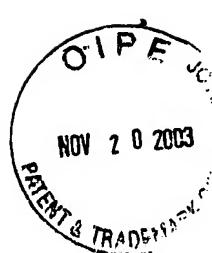


Fig. 7



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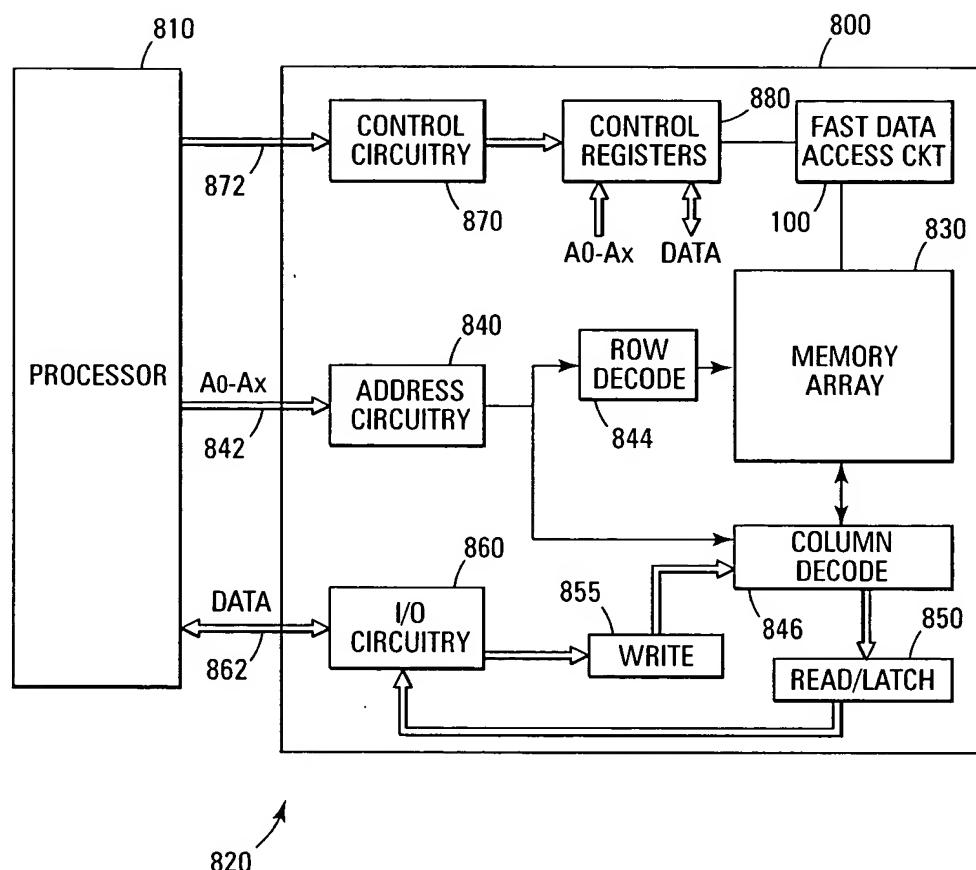


Fig. 8